

6.2 A 0.18 μ m CMOS Dual-Band UWB Transceiver

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UWB is recognized as one of the most promising techniques for short-range high-data-rate wireless applications such as wireless USB, AV streaming, and cable replacement [1]. The current implementations of UWB transceivers typically operate in the FCC low band of 3 to 5GHz [2-4]. There is a necessity to extend to the high band of 6 to 10GHz for two reasons. Firstly, to avoid the strong interference from other communication systems operating in the low band (e.g., WiMAX), some countries already considered to extend UWB to the high band and leave the low band as an option. Secondly, this could further improve transmission data rates without significantly increasing the power consumption. In this paper, a dedicated dual-band UWB transceiver architecture is proposed which can selectively work at low, high, or both bands of the UWB spectrum. Implemented in a 0.18 μ m CMOS process, it can achieve high data rate transmissions.

Figure 6.2.1 shows the dual-band UWB transceiver architecture. On the TX side, the parallel digital data bits (from a S/P converter) are converted to UWB pulses through pulse generators, which are then DSB upconverted to two bands centered at frequencies 4 and 8GHz, respectively. The dual-band signals are combined, pulse shaped, amplified, and applied to the antenna. On the RX side, the weak signal is amplified by an LNA, followed by SSB I/Q down-conversion mixers in the two bands, and then the downconverted signals are demodulated in parallel. The demodulated signals are converted to digital data by ADCs and then multiplexed to a serial data through a P/S converter. The frequency synthesizer generates 4GHz and 8GHz LO signals concurrently.

As shown in Fig. 6.2.2, self-synchronized modulation and demodulation schemes are proposed. The digital input data signals (a) and (b) are converted to spread-spectrum sequence (c) and (d) in parallel through pulse generators. Data signals (c) and (d) are upconverted by 4 and 8GHz LO, respectively, and then combined, pulse shaped, and amplified. The output of the driver amplifier (DA) is shown in (e). In the RX, signals (f) and (g) are the I/Q downconverted, squared, and combined versions of the received signals for the two bands, respectively. The low-pass filtered signal (applied to (f) and (g)) (h) and (i) can recover the transmitted data (a) and (b) correspondingly. This receiver does not require external synchronization since the LO phase uncertainty is eliminated by the SSB downconversion, squaring, and summation. Furthermore, the digital data signals, upconverted to two bands, are separated after the downconversion. Therefore this transceiver (TRX) allows concurrent operation of dual-band or one band at a time.

The transmitter circuits are also shown in Fig. 6.2.2. First, a high-speed XOR logic is used to act as a UWB pulse generator where one of the inputs is the digital data and the other is the 1GHz system clock. The generated pulse is then band-limited by a first-order RC filter. For the upconversion mixer, transistors M5 and M6 act as source followers to sense the large-swing input signal, and the generated current is steered through M1-M4 by LO signals. A high linearity is achieved with $1V_{pp}$ linear operation region for the RF input, and the two mixers are tuned to two bands separately. The inductor peaking (realized by L1 and L2) is used to expand the mixer bandwidth. The mixer achieves the following measured results: a conversion gain of -8dB, a noise figure of 8.2dB, and a -3dB bandwidth of 2.5GHz. The differential outputs of the mixer are converted to single-ended through a buffer without sacrificing the bandwidth, and the outputs from two mixers are combined together. Also shown in Fig. 6.2.2 is a DA. A wide bandwidth is achieved by combining two techniques, namely inductive shunt peaking (realized by L3, L4, and L6) and

inductive feedback (realized by L2 and L5). To reduce power consumption without sacrificing the gain, a current reuse technique is applied to the two cascoded transistors M1 and M2. The DA measures a gain of 10.5dB and a passband of 3 to 9.5GHz while drawing 5.4mA. Two stages of DA are cascaded in the TX to realize a pulse-shaping function that can comply with the FCC spectrum mask.

A measured pulse sequence at the TX output and its spectrum are shown in Fig. 6.2.3. The two parallel pseudo-digital data sequences are upconverted by the 4GHz and 8GHz LO, respectively. The emission pulse sequence appears as the addition of two upconverted pulses as shown in Fig. 6.2.3(a). The measured spectrum of the pulse sequences is shown in Figure 6.2.3(b), where the dual-band signals span from 3 to 5GHz and 7 to 9GHz and fit into the FCC spectral mask.

In the receiver, LNA is realized using a circuit similar to the DA in Fig. 6.2.2 but the input matching is designed to be less than -10dB across the 3 to 10GHz band. The mixer is basically a single-balanced Gilbert cell mixer with RC low-pass filtering at the output to remove the high-frequency components. The combined RF front-end achieves a voltage gain of 20.2dB, a noise figure of 5.6dB, and a -3dB bandwidth of 1.5GHz.

The low-pass filter is used to reject strong out-of-band interference and also suppress the leaked high frequency pulse signal. It is implemented by a 3rd-order active RC filter with cut-off frequency of 250MHz. The two-stage cascaded variable-gain amplifier achieves a dynamic gain from -10 to 45dB with a bandwidth of 300MHz. A low-pass feedback network is used to reject the DC offset with resulted cut-off frequency of 200kHz. The demodulator is implemented with two squarers and one nonlinear low-pass filter (NLPF), as illustrated in Fig. 6.2.4. Here, the input stage M7/M8 (M9/M10), common-mode input stage M17/M18 (M15/16), and current mirror M4/M13 (M3/M11) work as a squarer. The two squared currents are combined at the enhanced active load M1/M5 and M2/M6 to achieve a high gain. A 3-stage NLPF is used to extract different signal levels, where each stage is a common-mode-subtracted amplifier. Since the loading of the amplifier is an RC low-pass filter and a gate, thus the in-band DC level can be boosted while out-of-band noise and interference can be filtered out. Through this demodulator, the data bits can be recovered. The demodulator has input sensitivity of 150mV with 4.8mA current draw.

A separate ADC chip with a flash architecture and 4b resolution is adopted for further signal processing in baseband. An integer-N frequency synthesizer is implemented as shown in Fig. 6.2.4. The quadrature VCO operates at 8GHz and generates a 4GHz quadrature signal through a CML divider. The TSPC divider is optimized for high-speed operation and low power consumption. The measured phase noise is -100.15dBc/Hz at 1MHz offset for 8GHz LO with output power of -9.42dBm.

The transceiver IC is integrated in a 0.18 μ m CMOS process. The chips are directly mounted on a PCB and evaluated. The transmitted data pattern (at TX input), the measured emitted pulse pattern (at TX output), and the demodulated data pattern (at RX demodulator output), generated by directly connecting TX/RX and using an external LO for the purpose of testing, are shown in Fig. 6.2.5. The transceiver performance is summarized in Fig. 6.2.6. The chip micrograph is shown in Fig. 6.2.7.

References:

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- [4] Y. Zheng, Y. Tong, C.W. Ang, et al. "A CMOS Carrier-less UWB Transceiver for WPAN Applications," *ISSCC Dig. Tech. Papers*, pp. 116-117, Feb., 2006.

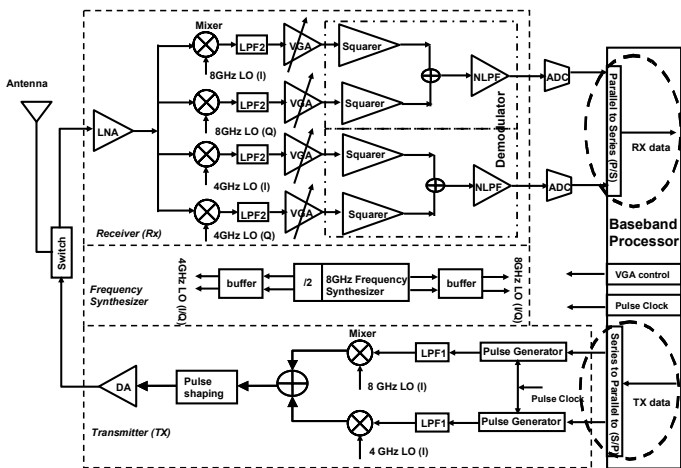


Figure 6.2.1: The dual-band UWB transceiver system architecture.

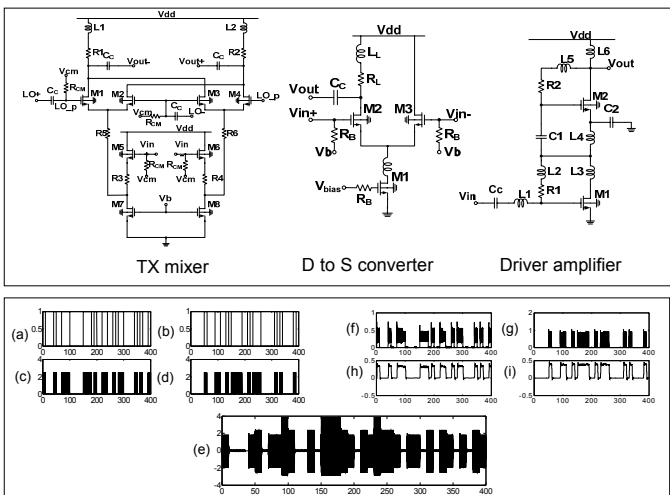


Figure 6.2.2: Pulsed TX circuits and modulation/demodulation scheme.

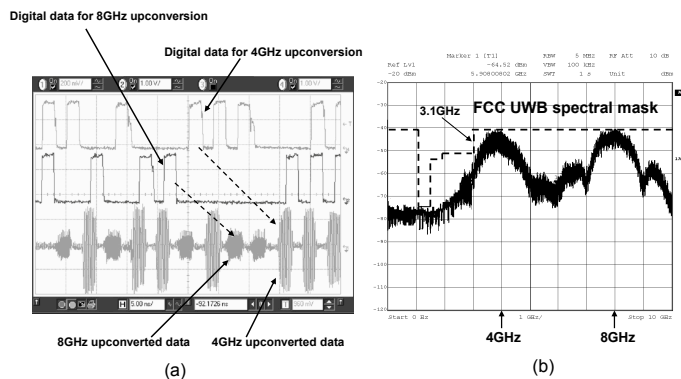


Figure 6.2.3: Measured TX pulses and spectrum: (a) time-domain pulses, (b) frequency spectrum.

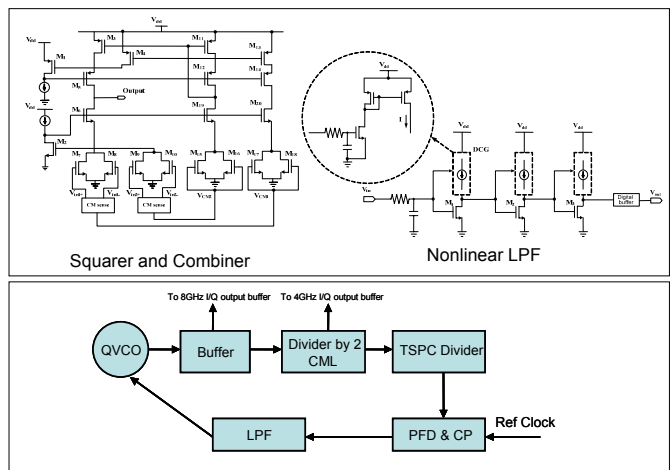


Figure 6.2.4: The demodulator circuit schematic and the frequency synthesizer diagram.

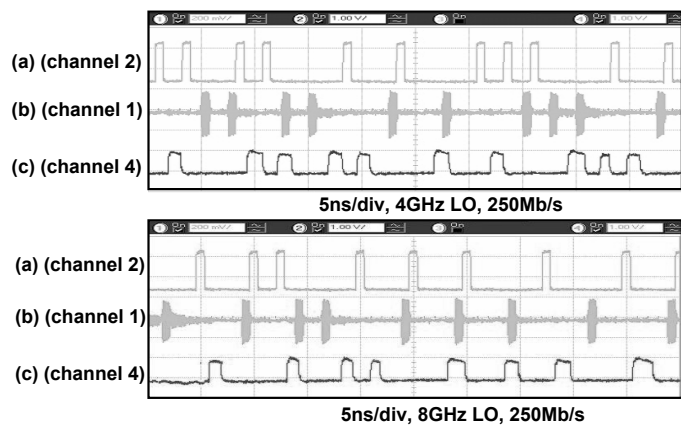


Figure 6.2.5: Measured RX outputs: (a) transmitted data pattern (b) emitted data pattern (c) recovered data pattern.

Receiver		Transmitter	
RX Noise Figure	8.6 to 9.4dB	Transmitted Power	-2dBm
RX Sensitivity	-79 to -76dBm	Digital data input range	1V peak-to-peak
IIP3 at Max Gain	-10.3dBm @ 4GHz -8.2dBm @ 8GHz	TX Bandwidth (-10dB)	2GHz for each band
IIP3 at Reduced Gain	-2.2dBm @ 4GHz 0.2dBm @ 8GHz	TX Current Dissipation	55mA
RX P-1 dB	-24dBm to -22dBm	TX data rate (Maximum)	300Mbps @ BER10 ⁻³ (400Mbps @ BER10 ⁻²) for each band
Selectivity (5.5GHz tone)	>30dB rejection	5-6 GHz notch	>20dB
RX Current Dissipation	76mA	Overall	
VGA Gain Range	-10 to 45dB		
LPF Bandwidth	250MHz		
Detector Sensitivity	150mV		
		Supply Voltage	1.8V
		Technology	0.18-μm CMOS
		TRX Die Size	16.7mm ²
		Frequency synthesizer	4GHz & 8GHz Quadrature

Figure 6.2.6: Summary of transceiver performance.

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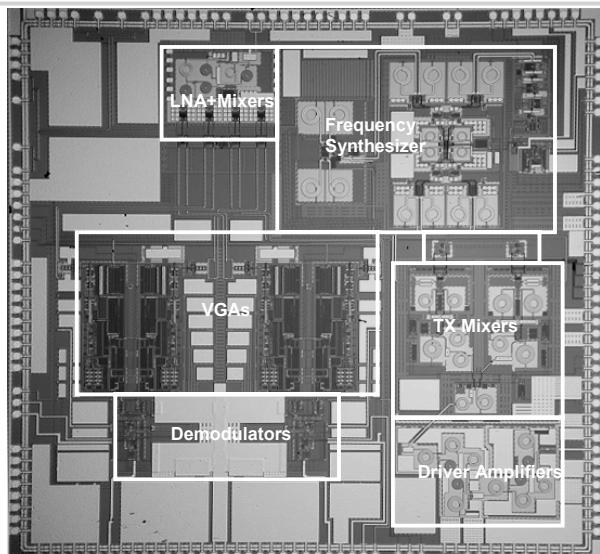


Figure 6.2.7: TRX chip micrograph.